## Amendments to the Claims

| 1. (Currently Amended) An electronic device for generating a clock signal for an            |
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| integrated circuit, the device comprising comprising:                                       |
| at least two clock generation elements (10, 20) arranged and configured to                  |
| generate a single clock signal at a clock output (18) in response to an input signal and to |
| operate in a mutually exclusive manner, the outputs of said clock generation elements       |
| (10, 20) being selectively connectable to said clock output (18),                           |
| the device further comprising,  |
| means (12) for receiving a data pattern (14) representative of a sequence of                |
| frequencies at which said clock signal is required to be generated,                         |
| means for receiving data representative of the next frequency in said                       |
| sequence,   |
| means for causing a clock generation element other than the clock                           |
| generation element generating the clock signal at the immediately previous frequency in     |
| said sequence to generate a clock signal at said next frequency,                            |
| means (24, 16) for causing the clock signal at the immediately previous                     |
| frequency in said sequence to be disconnected from said clock output (18), and              |
| means (24, 16) for causing the clock signal at the next frequency in said                   |
| sequence to be connected to said clock output (18); characterized in that the clock         |
| generation element (10, 20) being caused to generate a clock signal at each frequency in    |
| said sequence is independent of the value of said frequency.                                |
| 2. (Currently Amended) An electronic device according to claim 1, The electronic device     |
| as recited in claim 1, wherein the clock signal at the immediately previous frequency in    |
| said sequence is caused to be disconnected from said clock output (18) prior to             |
| connection of the clock signal at the next frequency in the sequence to said clock output   |
| <del>(18)</del> .   |
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3. (Currently Amended) An electronic device according to claim 2, The electronic device as recited in claim 1, wherein generation of the clock signal at said next frequency in said

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sequence is commenced prior to disconnection of the clock signal at the immediately previous frequency in the sequence from the clock output (18).

- 4. (Currently Amended) An electronic device according to any one of the preceding elaims, The electronic device as recited in claim 1, wherein connection of the clock signal at the next frequency in said sequence to said clock output (18) is caused to occur when said clock signal is low.
- 5. (Currently Amended) An electronic device according to any one of the preceding elaims, The electronic device as recited in claim 1, wherein disconnection of the clock signal at said immediately previous frequency in said sequence from said clock output (18) is caused to occur when said clock signal is low.
- 6. (Currently Amended) An electronic device according to any one of the preceding elaims, The electronic device as recited in claim 1, wherein said at least two clock generation elements (10, 20) comprise programmable ring oscillators.
- 7. (Currently Amended) An electronic device according to claim 6, The electronic device as recited in claim 6, comprising a variable programmable delay element for receiving data representative of the duration of a clock cycle of each frequency in said sequence.
- 8. (Currently Amended) An electronic device according to claim 7, The electronic device as recited in claim 7, wherein said variable programmable delay element causes the respective clock generation element (10, 20) to generate a clock signal at the required frequency.
- 9. (Currently Amended) An electronic device according to any one of the preceding elaims, The electronic device as recited in claim 1, wherein said data pattern (14) is derived from, or comprises, a series of requests for a change of frequency of said clock signal.

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- 10. (Currently Amended) An electronic device according to claim 9, The electronic device as recited in claim 9, further comprising an arbiter (22) for determining the order in which said requests are to be effected.
- 11. (Currently Amended) An electronic device according to claim 10, wherein said arbiter (22) orders said requests for action on a "first-come-first-served" a first-in-first-out basis.
- 12. (Currently Amended) An electronic device according to claim 11, The electronic device as recited in claim 11, wherein if two requests are received at substantially the same time, the arbiter (22) is arranged to randomly select the order in which action is taken on these two requests. these two requests are to be actioned.
- 13. (Currently Amended) An electronic device according to any one of claims 1 to 12, The electronic device as recited in claim 1, further comprising an event controller (24) for controlling the order in which said clock generation elements (10, 20) are caused to commence and cease generating a clock signal and/or the order in which said clock signals are connected and disconnected from said clock output (18).
- 14. (Currently Amended) An electronic device according to any one of claims 9 to 13, The electronic device as recited in claim 9, arranged and configured to temporarily disconnect all of the clock generation elements (10, 20) from the clock output (18), in response to a request to do so.
- 15. (Currently Amended) A method of generating a clock signal for an integrated circuit, the method emprising comprising:

  \_\_\_\_\_\_\_\_providing at least two clock generation elements (10, 20) arranged and configured to generate a single clock signal at a clock output (18) in response to an input signal and

to operate in a mutually exclusive manner, the outputs of said clock generation elements

(10, 20) being selectively connectable to said clock output (18),

18. (New) A clock signal generated by a method as recited in claim 15.